© INNOVATIVE RESEARCH THOUGHTS | Refereed | Peer Reviewed | Indexed
ISSN : 2454 – 308X | Volume : 04 , Issue : 06 | July - September 2018

A REVIEW ON HYBRID MULTIPLIER AND FUNCTIONALITY

Mamta Rani, Research Scholar, Department of ECE, IIET

Abstract: This paper discusses the digital system along with its basic functionality. In this paper the discussion has been made on existing researches related to Modified Booth Multipliers With a expected Fractional Product Array, Multiplier Reduction Tree with Logarithmic Logic Depth and Regular connectivity, Multiplication Acceleration Through Twin Precision Magnus, Implementation of a High speed Multiplication on SOC using Twin precision process. The multiplier and their working have been discussed in this paper.

Keyword: Multiplier, Fractional Product Array, Multiplier Reduction Tree, Twin Precision Magnus

[1] INTRODUCTION

It is not easy to create the digital systems. The original work is split into convenient subunits building blocks with the use of well-organized and efficient designers in any field. After that they utilize the standard subunits where there are acceptable. The building blocks are known as adders, registers, and multiplexers in digital hardware. It is presented by the logic theory that all digital operations may be reduced to elementary logic functions. It has been considered that a digital system made by the use of massive group of and, or, and not circuits. However incomprehensible outcomes are obtained. To resolve this problem it is required to shift 1 level up from the concept of gates.

Few candidates are:

(a) Shifting data from one portion from another of the machine.

(b) Selecting information from one of many sources.

(c) Routing records from a resource to single of several destinations.

(d) Moving data from one demonstration to another.

(e) Differentiate statistics arithmetically with another data.

(f) Manipulating data arithmetically or sensibly

By appropriate scheduling of AND, OR, and NOT gates it is possible to carry out all these operations. However scheming done at this stage would be difficult, extended, and contains error. For the execution of normal digital system operations it is required to develop building blocks. The inappropriate factors are restrained with the help of building blocks. They are proposed at a higher level.

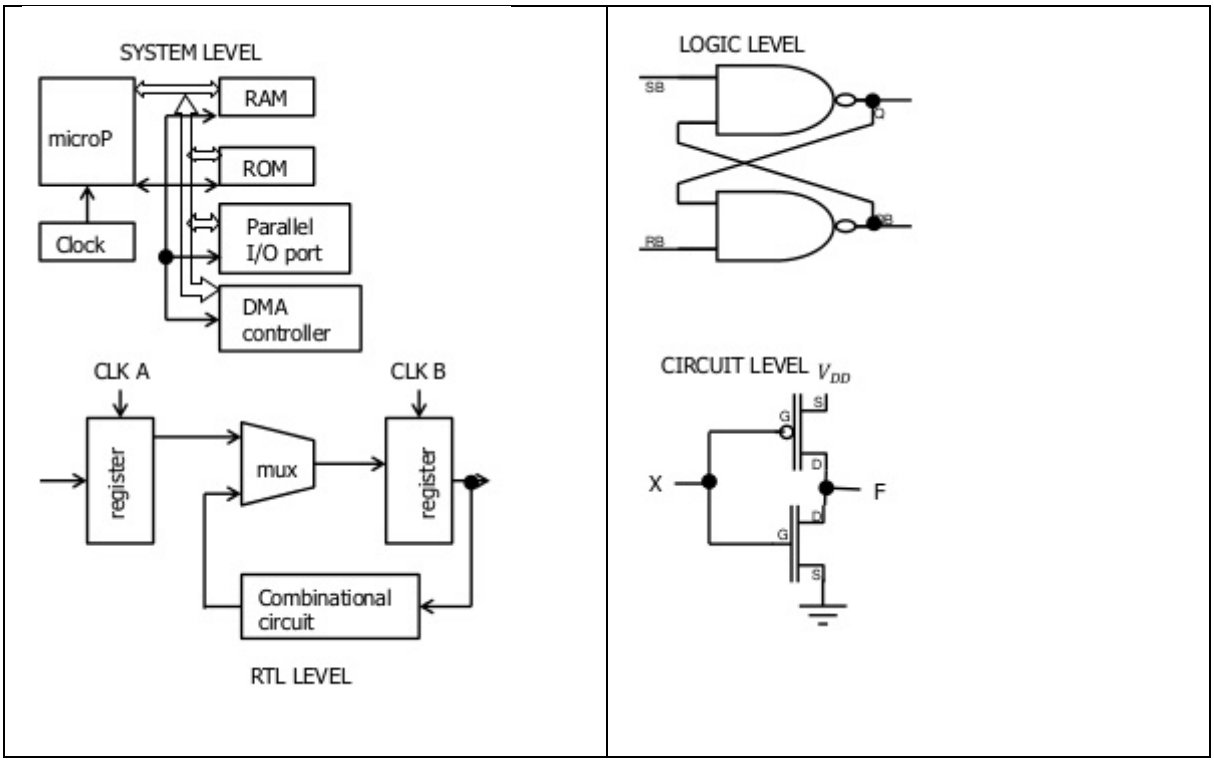

Fig 1 Digital system design

Design levels	Operand size	Processing time range(s)	Logic devices
System	Bytes/byte blocks	$10^{-3} and\ 10^{-6}$	Microprocessors/ microcomputers, memory devices, timers
RTL	Bits/bytes	$10^{-8}\ and\ 10^{-9}$	Decoders, encoders, multiplexers, registers, counters
Logic gate	Bits	$10^{-9}\ and\ 10^{-11}$	Basic logic gates, flip-flops, latches
circuit	Bits	$10^{-10}\ and\ 10^{-12}$	MOSFETs, BJTs

Table 1 Processing time range at different Design levels

[2] LITERATURE REVIEW

There have been several researches in field relevant field have been discussed in this section.

Modified Booth Multipliers With a expected Fractional Product Array. Shiann-Rong Kuang et al (2009): an uneven fractional product array is accomplished by the usual modified Booth encoding (MBE).It happens due to the presence of the additional fractional product bit at the slightest considerable bit position of all fractional product row. A straightforward way is put forward for the accomplishment of a standard fractional product array in which the partial product rows are less with minor overhead. In this manner we are able to reduce the complication of fractional product by reducing the area, delay, and power of MBE multipliers. The way which is put forward by us is also useful to normalize the fractional product array of post truncated MBE multipliers. Outcomes that

have been got after execution shows that a considerable progress in area, delay, and power consumption is attained by the anticipated MBE multipliers with a standard fractional product array really attain in comparison to the predictable MBE multipliers.

Multiplication Acceleration Through Twin Precision Magnus. Själander et al (2009) : the twin-precision procedure for integer multipliers is put forward by us. Power dissipation can be cut by the use of this procedure. It can be done the by accommodate a multiplier to the bit width of the operands being figure out. A better computational throughput is making possible by the use of this procedure. It is possible because this procedure allows us the parallel operation of a number of narrow-width operations which are to be figure out. It is also explained by us that it is possible to use this procedure to signed multiplier schemes, like Baugh–Wooley and modified-Booth multipliers. It is also made known that the twin-precision delay penalty is small (5%–10%) and a considerable drop in power dissipation (40%–70%) can be attained when working is done on narrow-width operands. It is also demonstrated by us that implementation time of a Fast Fourier Transform is reduced with 15% at a 14% cutback in information path energy dissipation. It can be done by stretching the multiplier of a general-purpose processor with the twin-precision scheme. All the transformation which are done by us depends upon the layout-extracted information from multipliers implemented in 130-nm and 65-nm commercial process technologies.

Multiplier Reduction Tree with Logarithmic Logic Depth and Regular connectivity: H Ericsson et al (2006): For utilizing the I integer multiplication is fresh partial product reduction circuit is put forward. The high performance multiplier (HPM) reduction tree has th 6 of layout of a simple carry save reduction array. It is a High speed low power Dada-style try having a low style tree having a worst-case delay which depends on the logarithmic(0(logN) of the word length N.

Implementation of a High speed Multiplication on SOC using Twin precision process. G. Swapnasri et al (2012): for digit multipliers the twin-precision procedure is put forward by us. Power dissipation can be cut by the use of this procedure. It can be done the by accommodate a multiplier to the bit width of the operands being figure out. A better computational throughput is making possible by the use of this procedure. It is possible because this procedure allows us the parallel operation of a number of narrow-width operations which are to be figure out. It is also explained by us that it is possible to use this procedure to signed multiplier schemes, like Baugh–Wooley and modified-Booth multipliers. It is also made known that the twin-precision delay penalty is small (5%–10%). A considerable drop in power dissipation (40%–70%) can be attained when working is done on narrow-width operands. . It is also demonstrated by us that implementation time of a Fast Fourier Transform is reduced with 15% at a 14% cutback in information path energy dissipation. It can be done by stretching the multiplier of a general-purpose processor with the twin-precision scheme. All the transformation which are done by us depends upon the layout-extracted information from multipliers implemented in 130-nm and 65-nm commercial process technologies.

High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree. Magnus Sjalander et al (2008): In high-speed multiplier circuits the method of modified-Booth is comprehensively used. A considerably superior performance of multiplier can be achieved by generating the reduced no. of fraction products with the use of array multipliers. The effect of reduced number of fractional products on overall performance is finite in models which uses

reduction trees with logarithmic logic depth . The method of Baugh-Wooley algorithm is unusual for signed multiplication. This method is however not accepted due to the reason that it is difficult to install on irregular reduction trees.It is demonstrated by us that for a variety of operator bit widths that, when used in 130-nm and 65-nm process technologies, the Baugh-Wooley multipliers display comparable delay, less power dissipation and smaller area foot-print than modified method.

[3] Multiplication

If a comparison is made between addition and Multiplication it is come in to notice that the latter is a vital fundamental arithmetic operation and less common operation with respect to addition. However it is crucial for microprocessors, digital signal processors and graphic engines. The demonstration of methods which are used for the design of different cells so that they fit into a larger structure is done by the use of Multiplication algorithms. A series of addition, subtraction and shift operations is performed for the execution of multiplication. It is very costly and slow operation. To resolve the problem of speed a high speed multiplier is used from which high speed multiplication is obtained. It is one of the fundamental functions deployed in digital signal processing (DSP). In comparison to addition and subtraction more hardware resources and processing time is required in multiplication function. An usual CPU gives a substantial amount of processing time for the realisation of arithmetic operations in computers, particularly multiplication operations.

[4] Multiplier

A multiplier is a hardware circuit dedicated to multiply 2 binary numbers are multiplied by the use of a hardware circuit which is known as multiplier. For the realisation of a digital multiplier a range of computer arithmetic methods can be used. Firstly the computing of a bundle of fractional products is done and after that fractional products are summing together in almost each and every method. It is related to the process which is used for the student of junior classes for conducting long multiplication on base-10 integers.

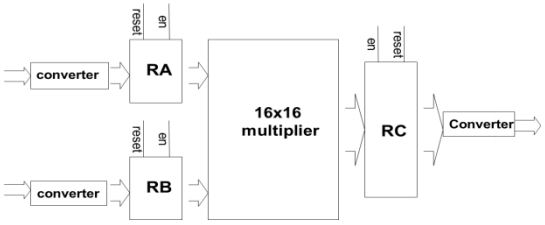

Fig 2 16x16 Multiplier

[5] Scope of research

Multiplication dominates the implementation time of most DSP algorithms is depends upon the multiplication. Therefore the requirement of high speed multiplier is essential. Most high for the realization of high data throughput all the DSP system whose performance are good have faith in hardware multiplication. Multiplication is an important fundamental arithmetic operation. The multiplier is a fairly large block of a computing system. The quantity of circuitry implicated is directly proportional to square of its resolution i.e., a multiplier of size of n bits has O (n2) gates.

REFERENCES

[1] Neeta Sharma, Dr. Ravi Sindal "Modified booth multiplier using Wallace structure and efficient carry select adder" in International Journal of Computer Application, ISSN No: 0975-8887, Vol.68-No.13, April-2013, PP. 39-42.

[2] Priya Sharma, Dr. Ravi Sindal "IMPLEMENTATION OF HIGH SPEED AND LOW POWER NOVEL RADIX 2 BOOTH MULTIPLIER USING 2248 BEC CONVERTER" in *National Conference On Recent Developments In Electronics (Ncrde 2013)*, IEEE Delhi Chapter in January, 2013.

[3] K.A.C. Bickerstaff, M. Schulte, and E.E. Swartzlander, Jr., "Reduced Area Multipliers,"

Intl. Conf. on Application-Specific Array Processors, pp. 478-489,1993.
[4] Prasanna Raj P, Rao, Ravi, "VLSI Design and Analysis of Multipliers for Low Power", Intelligent Information Hiding and Multimedia Signal Processing, Fifth International Conference, pp.: 1354-1357, Sept. 2009.
[5] Jagadeshwar Rao M, Sanjay Dubey," A High Speed Wallace Tree Multiplier Using Modified Booth Algorithm for Fast Arithmetic Circuits" IOSR Journal of Electronics and Communication Engineering (IOSRJECE), Volume 3, PP 07-11, Issue 1 (Sep-Oct 2012).
[6] Pouya Asadi, and Keivan Navi, "A new low power 32×32- bit multiplier", World Applied Sciences Journal 2 (4): 341-347, 2007.
[7] Purushottam D. Chidgupkar, and Mangesh T. Karad, "The implementation of algorithms in digital signal processing", Global J. of Engineering Education, vol.8, no.2 © 2004 UICEE Published in Australia.
[8] Michael Andrew Lia, "Arithmetic units for high performance processors", Thesis for degree of Master of Science, University of California, 2002.
[9] Soojin Kim, and Kyeongsoon Cho, "Design of high-speed modified Booth multipliers operating at GHz ranges", World Academy of Science, Engineering and Technology, 2010.
[10] Jagadeshwar Rao M, Sanjay Dubey," A High Speed Wallace Tree Multiplier Using Modified Booth Algorithm for Fast Arithmetic Circuits" IOSR Journal of Electronics and Communication Engineering (IOSRJECE), Volume 3, PP 07-11, Issue 1 (Sep-Oct 2012).
[11] Rabey, Nikolic, and Chandrasekhran, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Prentice Hall, pp. 586-594, 2003.
[12] Roy, Kaushik, Yeo, and Kiat-Seng, "Low voltage Low-power VLSI Subsystems", McGraw-Hill, pp.124-141.
[13] M. C. Wen, S. J. Wang, Y.N. Lin, "Low-Power parallel multiplier with column bypassing", ELECTRONICS LETTERS, vol. 41, no. 10, 12th May 2005.
[14] Weste, Neil H.E. Eshraghian, and Kamran, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd Edition, Pearson Education, pp. 345-356, 2005.
[15] A.D. Booth, "A signed binary multiplication technique", Quart. J. Mech. Appl. Marh., vol. 4, pp. 236-240,1951.
[16] O. L. MacSorley, "High speed arithmetic in binary computers", Proc.IRE, vol.49,pp. 67-91, 1961.
[17] L.P. Rubinfield, "A proof of the modified Booth‟s algorithm for multiplication", IEEE Trans. Comput., vol. C-24, pp. 1014-1015, Oct.1975.
[18] Razaidi Hussin, Ali Yeon Md. Shakaff, Norina Idris, Zaliman Sauli, Rizalafande Che IIsmail, and Afzan Kamaraudin, "An efficient modified Booth multiplier architecture", International Conference on Electronic Design, 978-1-4244-2315-6/08,2008 IEEE.
[19] C.S. Wallace, "A suggestion for fast multipliers", IEEE Trans. Electronics Comput., vol. EC-13, pp.14-17, Feb.1964.
[20] Parhami, Behrooz, "Computer Arithmetic: Algorithms and Hardware Designs", Oxford University Press 2000.
[21] Niichi Itoh, Yuka Naemura, Hiroshi Makino, Yasunobu Nakase, Tsutomu Yoshihara, and Yasutaka Horiba, "A 600-MHz 54 x 54-bit multiplier with rectangular-styled Wallace tree", JSSC, vol.36, no. 2, February 2001.
[22] Vojin G. Oklobdzjia, David Villeger, and Simon S. Liu, "A method for speed opitimized partial product reduction and generation of fast parallel multipliers using an algorithmic approach", IEEE Transaction on Computer, vol. 45, no. 3, March 1996.
[23] A. Dandapat, S. Ghosal, P.Sarkar, D.Mukhopadhyay, "A 1.2ns 16X16-bit binary multiplier using high speed compressors", International Journal of

Electrical and Electronics Engineering 4:3,2010.

[24] S.Shah, A.J.Kbalili,D.Al-Khabili, "Comparison of 32-bit multipliers for various performance measures", The 12th International Conference on Microelectronics Tehran, Oct. 31- Nov. 2, 2000.