



## PERFORMANCE ANALYSIS OF UNIFIED POWER FLOW CONTROLLER (UPFC) USING 3 LEVEL CASCADED H BRIDGE (CHB) INVERTERS WITH SPWM AND PI CONTROLLERS

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**Abstract** - Unified Power Flow Controllers are very much known for their versatility in independently controlling the Active and Reactive Power Flow in a transmission line<sup>1</sup> This paper proposes a unique combination of Advanced MLIs like Cascaded H Bridge Inverters in the Converters of UPFCs and a Control Strategies like PI CONTROLLERS for Alleviating the Performance Capabilities of UPFCs. This paper presents the detailed results showing the Improvement in Performance Capabilities of UPFC using the Proposed New Combination of CHB Inverters and Advanced Control Strategy over the Six Pulse Converters. Different Shunt Faults like LG (on Phase A) , LL (on Phases A-B) , LLG (on Phases A - B - Ground) and LLL (on Phases A-B-C) are created at bus number 4 . between bus 3-4 , and the capability of the PI Controller in restoring the system normalcy is also tested. The parameters used for analysing the controller's performance Settling Time. The test is carried out on a Standard IEEE 5 Bus System. The PWM Technique used is Sine Triangle PWM (SPWM). Simulations pertaining to the entire test procedures are done using MATLAB software.

Keywords – AC Transmission, FACTS, UPFC, IEEE-5 BUS System, Shunt Line Fault, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SPWM, PI Controllers, Rise Time, Settling Time.

### 1. INTRODUCTION

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the

utilities. An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self thinking machine. The Unified Power

Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2), connected in series with the Transmission Network. These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can independently generate and absorb real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude  $V_{pq}$  ( $0 \leq V_{pq} \leq V_{pqmax}$ ) and phase angle  $\delta$  ( $0 \leq \delta \leq \delta_{max}$ ) at power frequency in series with the transmission line voltage.

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### UPFC FUNDAMENTAL CONFIGURATION

Terminal Voltage Regulation is done with UPFCs wherein the required voltage of change required on the Transmission line say,  $\Delta V$  ( $V_{inj}$ ) , is injected either in-phase or in anti-phase mode with the existing voltage  $V_o$  on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say,  $V_{inj}$ , is injected in Quadrature with the Line Current.

Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of  $V_{inj}$  in an angular relationship with  $V_o$  to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

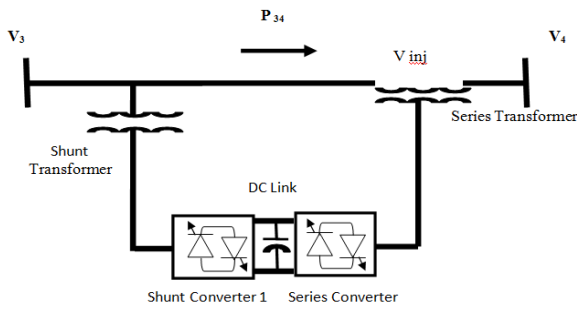


Fig.1. Basic Circuit arrangement of UPFC

POWER FLOW EQUATIONS OF UPFC CONNECTED BETWEEN THE BUSES 3 and 4

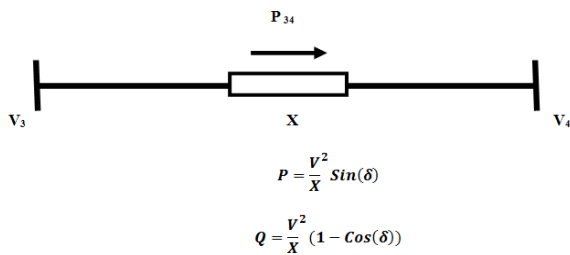


Fig. Power Flow Between Buses 3 and 4

$$P = \frac{V^2}{X} \sin(\delta)$$

$$Q = \frac{V^2}{X} (1 - \cos(\delta))$$

Fig.2. Circuit configuration between buses 3 and 4 (Power Flow Diagram )

Multi-Function Power Flow Control is obtained by simultaneously regulating the terminal voltage, series capacitive compensation and Phase Shifting action.

$$V_{pq} = \Delta V + V_c + V_\sigma \quad (1)$$

In the explanation that follows, the importance of using the PI Controllers in UPFC to enhance the Controlling Capabilities of UPFC are clearly explained. The UPFC incorporating a 3 Level CHB Inverter and a PI controller is tested for its improved performance on a Standard IEEE –5 Bus System. The UPFC is connected in the system between Bus number 3 and 4. The test conditions include (i) under voltage compensation (due to Increase in Inductive Load), (ii) over voltage compensation (due to Light load conditions or due to Capacitive over Loadings), (iii) Transient Stability Enhancement Capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG,LL,LLG and LLL Faults. The PI controllers are best known to be the fundamental Controllers in restoring Normalcy on a Power System Network. The immediate changes in the network conditions more importantly at the point of connection of the UPFC are detected and Appropriate Corrective

Actions are initiated by the PI Controllers. The UPFC Simulated in this paper mainly consists of a Cascaded H Bridge Inverter. The Advantage with the CHB Inverters is made use of in improving the Performance of the UPFC there by Improving the Protection Levels offered to the Power System Network when the Power System is subjected to Certain Adverse and Abnormal Conditions. One of the most widely used software MATLAB is used for simulating the said test conditions.

### The Cascaded H Bridge Inverter

One of the outcomes of the Research on the attempt to improving the Output Voltage of an Inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired Multi Level voltage is obtained by using different and separate voltage sources like Batteries, Fuel cells, Solar Photo Voltaic (PV) Cells, Capacitors etc., The major Advantages with Multi Level Inverters are their Minimum Harmonic Distortions in the Output Voltage, Low Electro Magnetic Emissions, High output to Input Ratios i.e., High Efficiency and More Importantly their High Voltage With Standing and Operating Capability and Modularity. The Multi Level Inverters have found great applications in the areas of Drive Controls, Uninterruptible Power Suppliers and Static Volt Ampere Reactive Generators (SVG).In general MLIs are divided in to three categories as Diode Clamped, Flying Capacitor and Cascaded Bridge Inverters. One of the advantages of MLIs over the Two Level Inverter is that they reduce the Common Mode Voltage causing the breaking leakage Current in Multi Drive Systems of High Power Ratings (Greater Than 250KW) based Vehicles.

### The Circuit Topology of Cascaded H Bridge Inverter

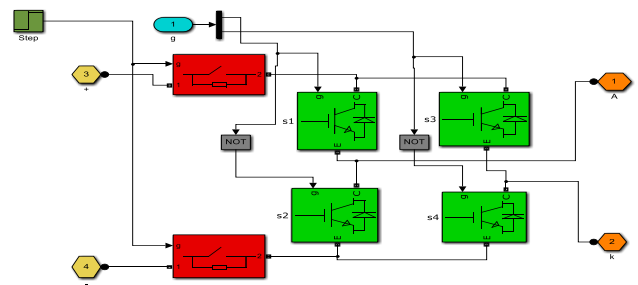


Fig.5. Basic Circuit of CHB Inverter used in this Simulation

The Fourier Series Output Voltage equation of the CHB Inverter (i.e., for a staircase waveform) is given by

$$V(wt) = \left(\frac{4V_{dc}}{\pi}\right) \sum_{n=1,2,3,\dots}^{\infty} (\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3 + \dots + \cos n\alpha_s) \sin nwt \quad (3)$$

Where

- $\alpha$  = the switching angle
- $n$  = harmonic number,



**V<sub>dc</sub>** = DC Supply Voltage of the Inverter

**s** = number of switching angles

Here the value of  $V(wt)$  is Considered as  $V_{inj} \sin \theta_{inj}$

For a given desired output fundamental voltage  $V(wt)$  it is required to find the switching angles  $\alpha_1, \alpha_2, \alpha_3 \dots \alpha_s$  in such a way that the total harmonic distortion is minimized.

The Magnitude of the Fundamental Waveform can be controlled by balancing the ratio of  $V$  and  $V_{dc}$  i.e.,  $V/V_{dc}$

The above ratio is called the Modulation Index denoted by  $M$

Therefore

$$M = \frac{V_{inj}}{V_{dc}} \quad (4)$$

Where **V<sub>inj</sub>** is the Maximum Value of the Inverters Fundamental Voltage, the Series Injected Voltage

From Eqn 2 ,  $V_1$  is the voltage output of the first H Bridge H1, and so on till  $V_n$  which is the output of the  $n^{th}$  cell Hn. In the initial stages each of the cells are supplied by individual DC sources later on it is experimentally shown that it is sufficient to have one of the cells fixed with a real DC source and the remaining can be supplied with capacitors. The change in redundancy in changing the sources is discussed in JingshengLiao in his paper CHB a re-examination. In this paper a Three Level CHB Inverter is used in the Series Converter of the UPFC. The operation of the Three Level CHB is explained in brief in the following session. The Switching pattern of the 3 level CHB is as depicted in the following table. The user specified output voltage of the CHB Inverter will be the Voltage that will be Injected through the Series transformer of the UPFC.

SWITCHING STATE				POLE VOLTAGE
Sw1	Sw2	Sw3	Sw4	V <sub>p-n</sub>
1	0	0	1	V
1	0	1	0	0
0	1	0	1	0
0	1	1	0	-V

Table.1. Switching States and Pole Voltages of 3 Level Cascaded H Bridge Inverter With Equal Voltages

The number of Voltage Steps or Levels that could be obtained by cascading X number of cells i.e., H Bridges is given by

$$N_{volt} = 2X+1$$

The Number of Levels of Voltages  $N_{volt}$  in case of CHB Inverters is always an Odd Number. Where as in case of Diode Clamped inverters it can be either even or odd.

The Total Number of Active Switches in a Cascaded H Bridge Inverter can be obtained from the following formulae

$$N_{act} = 6*(N_{volt} - 1)$$

In the Equation for Solution for Transfer of Power through the lines 3 and 4 , the magnitude of voltage and the corresponding phase angle at which it is to be injected in Series by the UPFC's Series device is calculated using the Newton Raphson Solution Method. The values thus calculated by the controller are generated using the UPFCs Converters. The Series Converter which consists of the Three Level Cascaded H Bridge Inverter plays a major role in producing the voltage of desired magnitude and phase angle i.e.,  $V_{inj} \sin \theta_{inj}$  . To Control the values of Voltage and Power Transferred on the transmission line we can control the values of  $V_{inj} \sin \theta_{inj}$  i.e., we can control the magnitude of  $V_{inj}$  alone ,Phase Angle  $\theta_{inj}$  alone or by simultaneously changing the values of  $V_{inj}$  and  $\theta_{inj}$  .

### THE PI CONTROLLER

THE PROPORTIONAL INTEGRAL (PI) CONTROLLER designed here is supposed to maintain the Output voltage and Power Flow to be intact with the reference values defined by the user.

The PI controllers used here are Two in number The DC Capacitor Voltage Controller (Shunt controller)

The Injected Voltage Controller (Series Controller) The Following PI Controller takes inputs from the IEEE 5 bus system's 4<sup>th</sup> Bus i.e., the Load Bus for us, and the DC capacitor voltage at the DC Link , continuously and compares it with the Reference values defined by us and Processes it for further correction initiation action by the Shunt Converter. The Capabilities of the PI Controller Tested here are for the problems that occur at the Bus 3-4, like (i) change of Nature of Load from Highly Inductive Dominating to Highly Capacitive Dominated (ii) during the Occurrence of faults like LG, LL, LLG and LLL It is observed that the PI controller within its controllable Capabilities is able to maintain proper Voltages at the DC bus also.

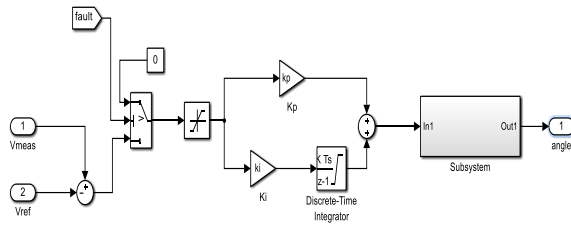


Fig.7(a).

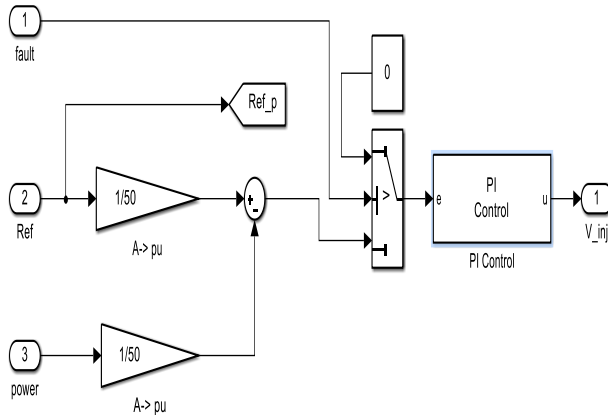


Fig7.(b)

Fig.7.(a) and (b) : The Injected Voltage Controller

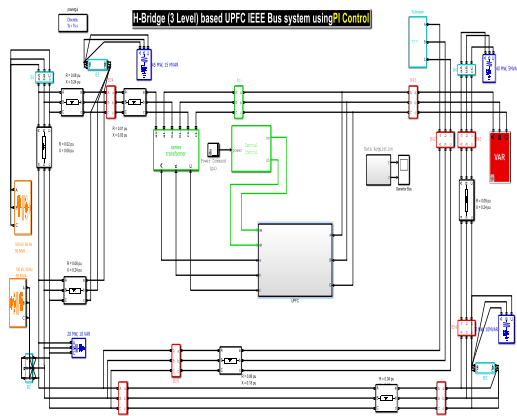


Fig.8. UPFC consisting of Three Level CHB Inverter connected between Buses 3 and 4 in an IEEE 5 Bus System

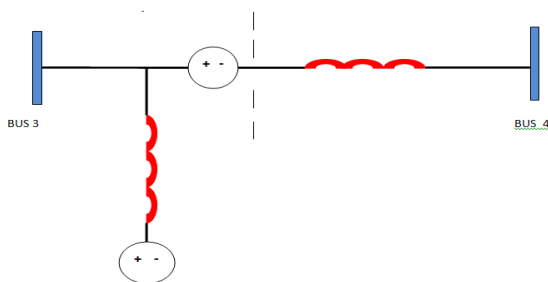


Fig.9. Equivalent Circuit of UPFC connected between buses 3 and 4

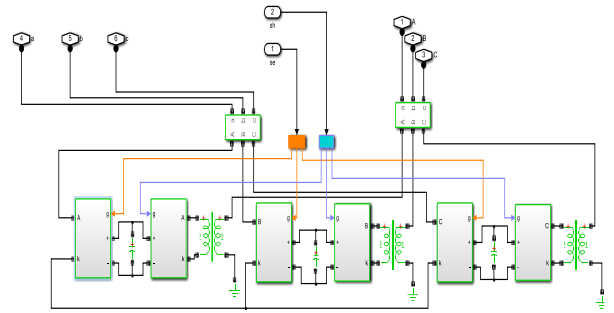


Fig.10. The Tree level Three Phase Cascaded H Bridge Inverter based UPFC Circuit Connections

**THE PI CONTROLLERS FOR THE SHUNT AND SERIES SYSTEMS OF THE UPFC**

The Proportional Integral (PI) Controllers are best known for their simplicity in design and effectiveness in response times taken for solving the power system voltage correction and power flow problems. The entire functionality of the UPFC is controlled by the PI controllers. Each of the two systems i.e., the Shunt Controller and the Series Controller has one PI controller each .

The PI controller of the Shunt system works to maintain proper value of Shunt current and the DC Voltage across the capacitor.

The PI controller of the Series System works to produce the required Magnitude and Phase Angle of the Series Injected voltage

The following Figure shows the two PI Controller System connections used

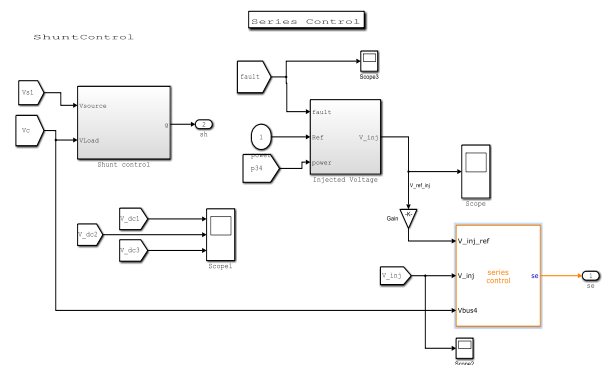


Fig.11. The Series and Shunt Controllers of the UPFC

**THE SHUNT CONTROLLER**

The Shunt Controller is designed to take the reference from an external reference , Vreference , and the Load Voltage , Vload (later converted to Vmeas ) , at bus number B4.



The output of the shunt PI Controller is the reference phase angle value of the Quadrature Axis Component of the Shunt Current ( $I_{q\_ef}$ ). This value of the Angle reference is utilised by the Controller's Control Signal generator section to generate the required reference angles for the Pulses triggering the Shunt Converter.

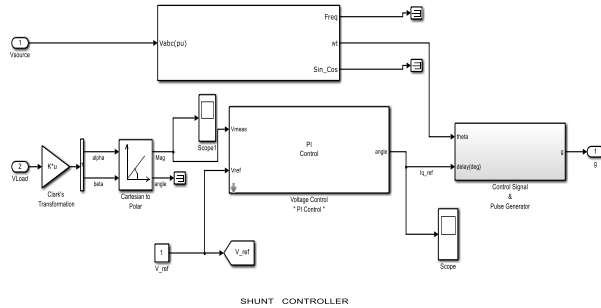


Fig.12. The Internal Structure of the PI Shunt Controller

### THE SERIES CONTROLLER

The Series Controller is also incorporated with a PI Controller. The basic inputs to the PI Controller in this section are the reference series Injected Voltage  $V_{inj\_ref}$ , the voltage at bus number 4,  $V_4$ .

The Series Voltage injector monitors the Voltage ( $V_{load}$ ) on the Transmission Line 3-4 and the Power that is transferred from bus 3-4 ( $P_{34}$ ). These values are continuously compared with the reference values and correction actions to be taken by the Series Voltage Injector Converter are initiated.

The controller and Pulse generator takes in the Existing (Measured) and reference values of voltages as Inputs and produces Pulses accordingly. The calculations pertaining to the production of Pulses are shown in Figure.....

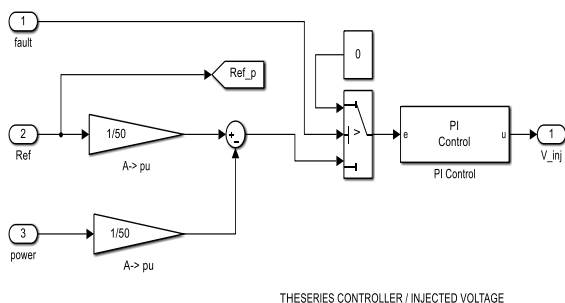


Fig.13. The Internal Structure of the Series Controller / Series Injected Voltage Controller

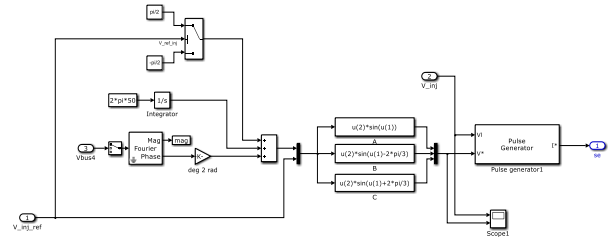


Fig.14. Internal Structure of the Series Injected Voltage Controller Pulse Generator Circuit

### THE OUTPUTS - RESULTS AND DISCUSSIONS

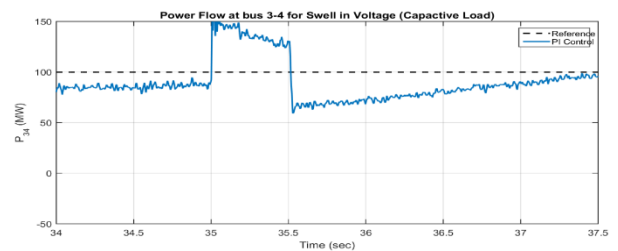


Fig.15. The Power Flow diagram at Bus 3-4 for Swell in Voltage due to Addition of Capacitive Load

The above figure 15 indicates the performance of the UPFC in restoring normalcy after sudden change in loading conditions from Normal to Capacitive is applied. Here a capacitive load of 100 MVAR magnitude is imposed in addition to the regular load of (40MW + 5MVAR-Inductive) at bus number 4. When the Capacitive Load Is Switched On at 35<sup>th</sup> Second, the Total Power Carried By the line increased to 150 MW. And when the Capacitive load is switched off at the 35.5<sup>th</sup> second, the Power level suddenly falls to 52MW. This Swing in the system, if allowed to persist for longer durations, will resort to Severe damages of the system components and may eventually lead to collapse of the entire electrical network including De Synchronization and Blackout. The Unified power Flow Controller is a very versatile component which gives utmost robust support during such swings also. Here with the help of the 3 Level Cascaded H Bridge Inverter based Series Converter, the UPFC injects the remaining amount of deficit power of 48 MW and Simultaneously the Proportional Integral (PI) Controller Manages the Swing Level viz., Peak Over Shoot, Rise Time and Settling Time by appropriately Varying the Series Injected Voltage i.e., The impact of sudden changes in Loading or Sudden Loss of Excess capacitive load is overcome by appropriate Magnitudinal Changes and Phase Displacements of the Injected Voltages by the Series Voltage Injected. It is observed from the above figure, that the UPFC could regain the Normalcy or Rated Value of 100 MW with in a time span of 2.0 Seconds from the instant of Switching off the Capacitive Load i.e., from 35.5 seconds to 37.5 seconds.

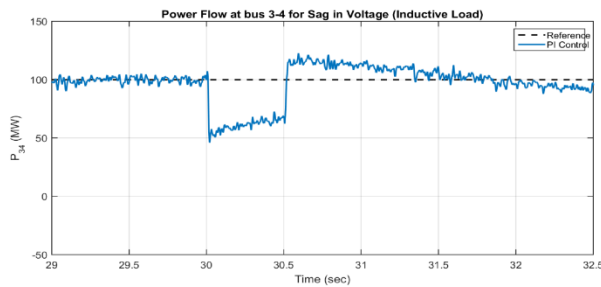


Fig.16. The Power Flow diagram at Bus 3-4 for Sag in Voltage due to Addition of Inductive Load

The Above figure indicates the ability of UPFC to restore normalcy after sudden changes in Inductive loads. An excess load of 100 MW apart from the regular Load of 40MW is added at bus number 4 .The load is suddenly added to the system at 30<sup>th</sup> s oscillations are brought to a stable state within a period of 2.5 s after a sudden loss of 100MW of Inductive load at bus number 4.

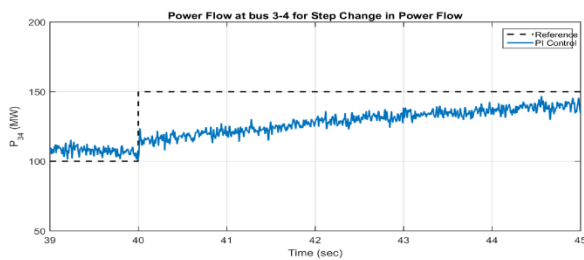


Fig.17. The Power Flow diagram at Bus 3-4 for changes in the Reference Values

The above figure indicates the capability of the UPFC in Alleviating the Power Transmission capabilities of the UPFC. The reference value of Power to be transferred is set to 150MW instead of 100MW. The Change in the reference values are gradually compensated by the UPFC within a period of 5 seconds from 40 to 45 seconds.

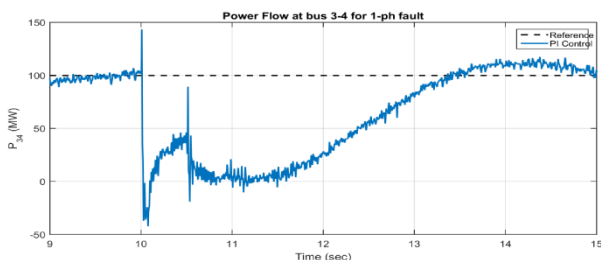


Fig.18. The Power Flow diagram (indicating restoration of Normalcy after fault ) at Bus 3-4 for an LG fault at Bus No 4

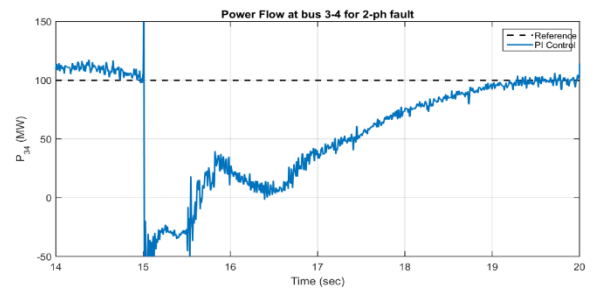


Fig.19. The Power Flow diagram (indicating restoration of Normalcy after fault ) at Bus 3-4 for an LL fault at Bus No 4

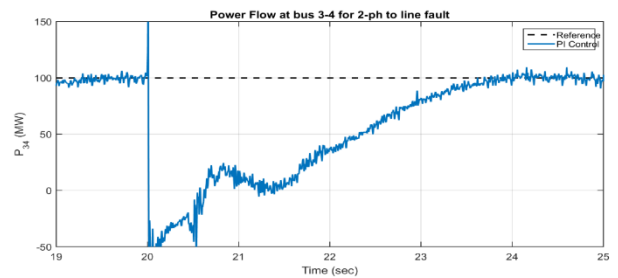


Fig.20. The Power Flow diagram (indicating restoration of Normalcy after fault ) at Bus 3-4 for an LLG fault at Bus No 4

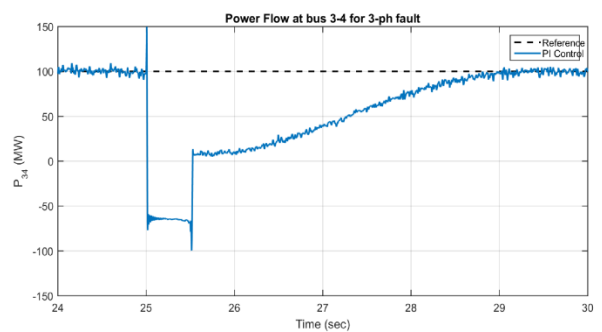


Fig.21. The Power Flow diagram (indicating restoration of Normalcy after fault ) at Bus 3-4 for an LLL fault at Bus No 4

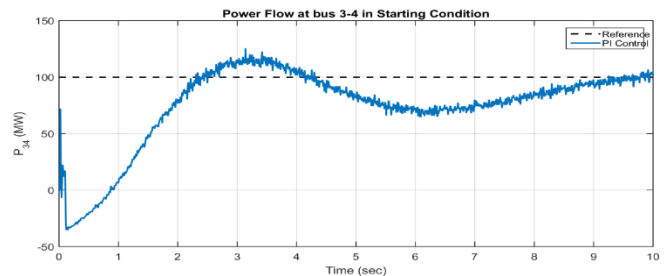


Fig.22. The Power Flow diagram at bus no 3 -4 during starting condition

**SETTLING TIME**



S.No	TYPE OF DISTURBANCE	DURATION OF DISTURBANCE IN SECONDS	SETTLING TIME IN SECONDS (EXACT TIME)
1	VOLTAGE SAG	0.5 (30 to 30.5)	1.70 (at 31.75)
2	VOLTAGE SWELL	0.5 (35 to 35.5)	2.0 (at 37.5)
3	SWITCHING ACTION STEP CHANGE FROM INDUCTANCE TO CAPACITANCE	Instant (at 40 th Sec)	5.5 (at 45.5)
4	LINE TO GROUND FAULT	0.5 (10 to 10.5)	4.5 (at 15 <sup>th</sup> SEC)
5	LINE TO LINE FAULT	0.5 (15 to 15.5)	4.2 ( at 19.7 SEC)
6	LINE TO LINE TO GROUND	0.5 (20 to 20.5)	3.5 (at 24 SEC)
7	THREE PHASE FAULT	0.5 ( 25 to 25.5)	3.5 ( at 29)

Table .2. Response Times of UPFC for Different Conditions

The above Table 2 indicates clearly the capability of UPFC in restoring the Power Flow in the transmission lines to a stable state when the Power System Network is subjected to different transient states. The CHB Inverter extends its strong voltage support and the PI controller helps in quick restoration of stable state following a Disturbance.

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**APPENDIX**

**IEEE-5 Bus System**

NUMBER OF LINES = 7  
 NUMBER OF BUSES = 5

In all these BUS DATA’s type-3 indicates slack bus, type-2 indicates PQ / load bus, type-1 indicates PV / generator bus.

**LINE DATA**

SB	EB	R (p.u)	X (p.u)	Ys	Tap
1	2	0.02	0.06	0.03	1
1	3	0.08	0.24	0.025	1
2	3	0.06	0.18	0.02	1
2	4	0.06	0.18	0.02	1
2	5	0.04	0.12	0.015	1
3	4	0.01	0.03	0.01	1
4	5	0.08	0.24	0.025	1



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