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# Simulation and Analysis of Single-Electron Transistors (SETs) Using TCAD and Virtuoso Framework: Advancing Low-Power Nanoelectronics

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**Abstract**
Single-electron transistors (SETs) are pivotal in advancing nanoelectronics due to their extremely low power consumption and unique electron transport characteristics. This research paper presents a comprehensive simulation and analysis of SETs using Technology Computer Aided Design (TCAD) and Virtuoso framework. We explore the device layout, including intrinsic type channel structures and material specifications, and simulate the electrical behavior of SETs under various conditions. Our findings highlight the influence of gate voltage, electron mobility, and temperature on device performance. Additionally, we discuss the Coulomb blockade effect and its impact on SET operation. The results demonstrate the potential of SETs for low-power digital circuit applications, emphasizing their significance in future nanoelectronic circuits.

***Keywords:*** Single-electron transistor (SET), Nanoelectronics, TCAD, Virtuoso framework Coulomb blockade, Electron mobility, Device simulation, Low power consumption, Quantum tunneling

## 1. INTRODUCTION

Highly multifaceted electronic systems can be achieved by successful downscaling of devices and encroachment of process technologies. The microelectronics industry had enhanced the circuit performance by dwindling the geometries of the transistor over four decades. Computer recreations have materialized as a smart method to assist process and device engineers for finding a best possible process. Simulation programs serve as a logical tool to achieve better understanding of process and device simulation.

It is also possible to recognise diversions after the arrangement section has been completed in order to advance the guarantees that have been established for expansion. Displaying and reenacting single electron semiconductors has been a subject of research that has been operating for quite some time. In order to form SETs, the Monte-Carlo model has been used extensively. For the first time in 1985, Dimitri Averin and Konstantin Likharev presented the SET test frameworks known as SIMON and MOSES. These two frameworks have since been the most widely used. The MonteCarlo method is used by MOSES and SIMON in order to gain the regular number of electrons in Coulomb Island respectively. In any event, they are not appropriate for the evaluation of extended circuits because they do not support CMOS/SET crossover circuits, they are not enough flavor-suited, and they are not suitable. In an easy manner, SENECA and other testing methods solve the expert requirement for the population probability of Coulomb Island. In spite of the fact that the aforementioned methods provide an accurate replica, they need a significant amount of framework computing due to the requirement to monitor the development of each coulomb island. TCAD (PC-Based Plan Development) units, which combine cycle exhibiting and device showing devices linked with cutting-edge frameworks organisation and development writing computer programmes, are ready to be purchased from a wide variety of remarkable dealers in a short amount of time. Solvers of important fractional differential equations (PDEs) are the devices that are now being used for showcasing devices. Each of these devices is designed to deal with a certain PDE framework that is associated with semiconductor displays. Two different approaches may be used with TCAD: In the first step, an analytical simulation of the device's

design is performed. This simulation offers predictions about the various processes that may be performed, how the device will function, and how the circuit will operate. Utilising exploratory information for the purpose of modifying the models that are already existing in the test framework and utilising it for the headway stage is the strategy that has been developed as a consequence.

SET has proved the achievement of very low power consumption caused by its low voltage operation and extremely low currents caused by electron transport in discrete fashion in a one by one manner. The frequency and time delay reactions of SETs are observed to be quick because of electron transport by tunneling phenomena.

Using the energy that is charged, single electron devices are able to regulate the vehicle that individual electrons are travelling in. The components that comprise it are a source, a channel, and the section crossing point, with a Coulomb in the middle of the assembly. The source, Coulomb Island, and the channel are all separated from one another by the intermediary that is the entrance crossing sites. Through a process known as tunnelling, electrons are transported across the apparatus in a sequential manner to each component. Due to the fact that the Coulomb Island charge energy only permits the tunnelling of a single electron at a time, the streams that are experienced in the single electron device are considered to be unstable.Unlike other devices, the single-electron device has a number of interesting qualities that set it apart from other devices. These characteristics include its very low power consumption, its adaptability to the nanoscale range, and its strong resistance for a limited amount of charge. One of the most important requirements for the construction of the gadget is that its components be positioned in the correct manner.

By virtue of the fact that the quantity of extra electrons is not linked, single electronic circuits that consist of anything like an island have a distinct but infinite number of states. It is abundantly clear that the Coulomb bar is directly responsible for the existence of a greater number of flood carriers, which are notably masked and more difficult to comprehend. The adoption of an all-inclusive plan is justified by the fact that it starts with the initial state and calculates the passage speed for every possible modification. This is due to the fact that it is difficult to separate the most probable states from an inconsistent scheme. As a measure of the no connection for the chance of the condition of distinct states that have showed up at these rates as a change, these paces are used as a gauge. Generally speaking, a high change rate indicates a high probability state, and the contrary is also true. In the event that the charge is found to fall under a certain edge, the state will not be taken into consideration. The fundamental requirement is decided via all of the states that have maintained the cutoff test. New states are related to the arrangement of crucial states in the subsequent cycle, and the circuit is shown more accurately as a result. The process that is being described here is referred to as an excursion across state space, and it involves commencing with the arrangement of states that have been discovered in a proactive manner and then travelling to other states inside state space.

## 2. DEVICE LAYOUT

Single electron transistor can be considered the most important single electron device. It demonstrates a few intriguing highlights in its electrical characteristics and behavior so it is the most considered device in single electron devices. It comprises two single-electron channel junctions which are slotted in a single conductive island sandwiched between them. Each single one of these channel junctions can be thought of as a capacitor, but with a thinner coating of protective material. To control SET conductance, two gates are appended to the island through a thicker layer of protective material to anticipate tunneling through it. The goal of study and design of a device is its applicability. The designed SET in this thesis can be used in various digital circuits design with its unique advantage of low power consumption. The reduction in power can be used at different levels. At circuit level reduction in power provides flexibility in design. For digital circuit design a good understanding of inverter is needed. By

understanding the operation and characteristics of an inverter the concept of any logic gate can be easily understood. As the basic building block of digital design is an inverter so an inverter is designed using SET. Fabricated single electron inverter output changes from high state to low state when input is added with fraction of electron. An inverter is logic circuits.

Single Electron Transistor with an intrinsic type channel structure of silicon oxide ($SiO_2$) and the spacer built on a SOI wafer is revealed in fig. 1. An island of length and width 0.015 µm and 0.006 µm respectively are divided with source and drain regions with the same material. The source and drain regions are also doped with doping concentration of $1x10^{20}cm^{-3}$.

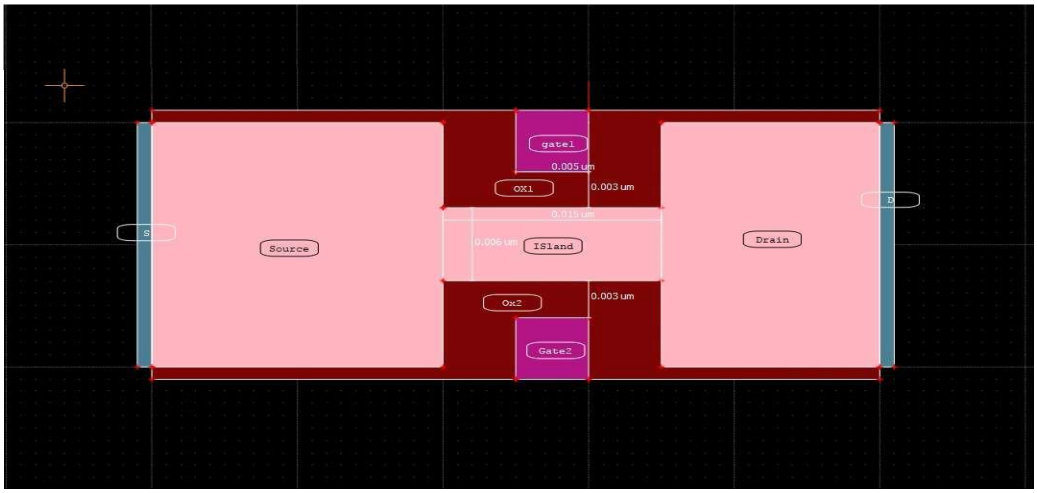


**Fig. 1 proposed layout of single electron transistor**

For the arrangement of the device, two entryways G1 and G2 whose length and width is 0.005 µm each with the oxide thickness from the entrance to the island is 0.003 µm are considered. The wall spacers of district 8*5nm2 on the different sides of entryways are expected to reduce the degrees to be accountable for doorways. Along these lines, to have power with entryways, two doorways are shaped to control the approaching of Coulomb Island. The coulomb island is specific on a two layered silicon island with tunneling limits. Built environments are used to create quantum effects with potential obstacles.

Control entrances and source/channel regions are self-changed in accordance with obliterate the freeloading mass part is used in the proposed structure. The coulomb island quantum-bits are also dove in the proposed structure. The components of the entire plan showed in the Table 1. We have found that an island/channel estimation of around 5 nm is expected for the charging energy thought. Thusly the SET creation development ought to be ready for making a channel of something like 5-10 nm size (width for circle shaped, line length in rectangular channels). The gadget's charging energy should be more noteworthy than its nuclear power to notice the Coulomb barricade impacts in a solitary electron gadget.

**Table 1 Particulars Of Top View For The Proposed Structure**

| Region | Channel | Gate | Oxide Thickness | Spacer | Source/Drain |
|---|---|---|---|---|---|
| Material used | Intrinsic Type | Poly Silicon | - | Silicon Oxide | Silicon |
| Doping Concentration | 1 e+14 | - | - | - | 1 $e^{+20}$ |

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| | | | | | |
|---|---|---|---|---|---|
| Dimensions | $6\times15nm^2$ | $5\times5nm^2$ | 3nm | $8\times5nm^2$ each side | $20\times20nm^2$ |

The layout with the material used in the structure is shown in the Fig. 2. It consists of five parts namely source, gate1, gate2, island and drain as shown in the figure which is called as device mess. In this structure, the gates are designed with n channel polycrystalline silicon since it pedals the potential of Coulomb Island. One free electron is created for each added donor atom. If donor impurity concentration is $N_d$ then concentration of free electron will also be same. The value of drain voltage is kept small because we are using a 2nm channel and have to show minimum conductance.

It possibly will also be used to prevent the low activation energy of Aluminum to be in motion around the next layers where it could have an effect on the band levels. The material used in proposed layout is shown in figure 2. This is called as device mesh. The main parts are Source, gate, island, Si dot and Drain. In this structure the gates are designed with n channel polycrystalline silicon to regulate coulomb island potential. Drain and source region are isolated by formation of island .To draw the device structure visual TCAD is used.

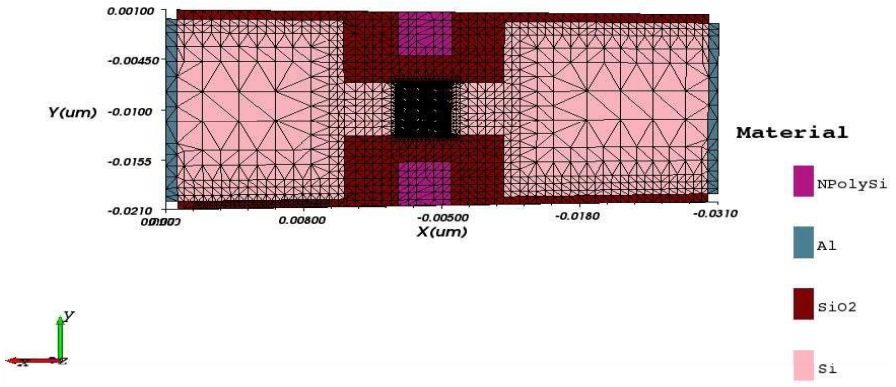


**Fig. 2 Device Mess**

For gate characteristic, the drain current works as an element of the gate voltage. Here the gate power, deplete voltage, the source and substrate (back gate) voltages are specific and the device temperature is at 300 K (room temperature operation).

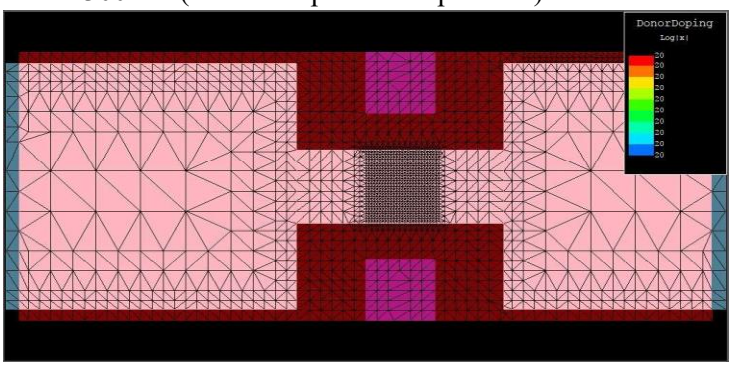


**Fig. 3 donor doping**

The doping of the giver is shown in Figure 3, and it is uniform throughout the whole circuit. There is a complete and total ionisation of the giver particles as soon as they are introduced into the semiconductor material. If the concentration of the pollutant (for example, phosphorus) in silicon is ND, which is the centralisation of free electrons, then each supporter atom will produce one free electron. The value of ND is equal to 10 times 20 cm-3.

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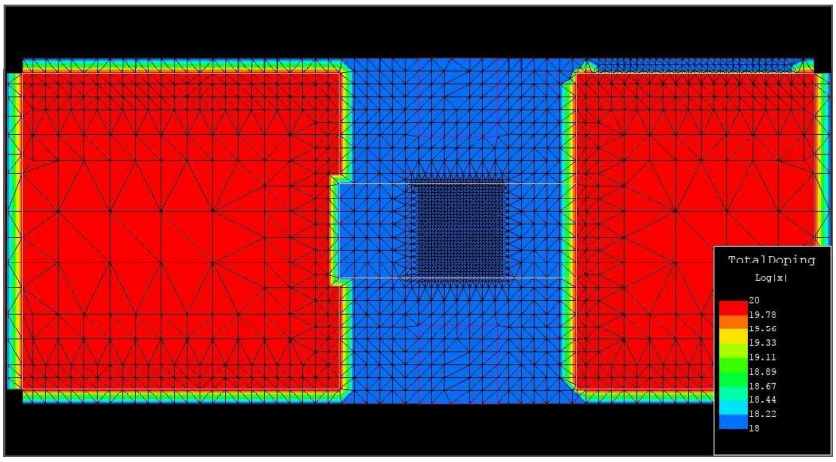


**Fig. 4 total doping**

A barrier that enables you to alter the number of electrons that are contained inside a quantum speck within a certain range is referred to as the all out doping thickness. The range of doping is determined using a logarithmic scale that ranges from 18 to 20. Figure 4 illustrates the all-out doping, which ranges from significant amounts of 18 to 20 at a variety of levels.

**3. DEVICE SIMULATION**

In order to duplicate the process, the parameters of the technique and the features of the device device SET are used. In accordance with the illustration in figure, the gadget SET is reserved after the playback cycle has been finished. The source, the channel, the entrance, and the substrate are the four cathodes that cannot be confused with one another. A never-ending supply of the game plan, also known as the all-out plan (complete semiconductor), is being safeguarded and will be used for the characteristics of the contraption. Contraption pantomime involves selecting the features of the machine, which are comparable to the attributes of the entranceway and the characteristics of the channel. After then, the features of the semiconductor device with a single electron are envisioned at that moment. For the purpose of reenacting the contraption, the facts that corresponds to the outcomes of the collaboration proliferation are used. The process propagation involves the relocation of the setup so that it may function as data. As shown in the diagram, the plan is made up of five different components: the island, the gate1, the gate2, the source, and the channel. In the study that is being presented here, several apparatuses, such as Visual TCAD and Virtuoso Test framework, are used in order to test the introduction of single electron semiconductor. To replicate the electrical and actual one-of-a-kind characteristics of the single-electron semiconductor, the Virtuoso framework, which is a numeric semiconductor device test framework, is used. Both the portable and stationary charges are responsible for picking up the electrostatic ability of every different semiconductor device. Taking into consideration electrostatic potential It is the state of the poisonous material that is utilised to determine the adaptability of the carrier. The equations that make up the system that is considered to be float diffusionThere are zero equations that are composed of the Poisson condition.

$$\nabla \cdot (\epsilon \nabla \phi) = -q(p - n + C) \quad (1)$$

the continuity equations for electrons and holes

$$\nabla J_n - q\frac{\partial n}{\partial t} - qR_n \quad (2)$$

$$\nabla J_p + q\frac{\partial p}{\partial t} - qR_p$$

and the current-density equations for electrons and holes

$$Jn = -q\mu_n n\nabla\phi + qD_n\nabla_n \quad (3)$$

$$Jp = -q\mu_p n\nabla\phi - qD_p\nabla_p$$

where $\phi$ is Rn and Rp are two abilities that may be regarded as depicting the age and recombination of carriers. The electrostatic potential, n and p are the electron and hole densities, respectively. C is the total density of ionised donors. Jn and Jp are the current densities. Rn and Rp are also able to be considered as skills that portray the recombination of carriers. The Dn and Dp are the limitations that are determined by the material; they are not fixed. Numerical game plans of this course of action of circumstances, maybe enhanced by energy balancing conditions, with an electronic variable and opening temperature (hydrodynamic model), incorporate the key purpose of obsolete gadget exhibiting. As the conventional assumption of single devices demonstrates, the correct operation of a SET device requires the utilisation of two different frameworks on its part. The first is that channel safeguards should be superior to quantum checks in order to successfully catch an electron that is located on an island. Second, the charging force of the island capacitance should be favoured over continuous nuclear power in order to avoid electron burrowing caused by thermionic production. This is intended to prevent the formation of electrons. The properties of the veered off tunnel securities will clearly influence the entry pace for the single electron semiconductor equipped with imbalanced section crossing points. Additionally, conflicting entry capacitances will change the designation of the tendency voltage across tunnel convergences, which will have an indirect impact on the section rate. The burrowing speed at source and deplete junctions is greater. This is due to the fact that channel blockage is more widespread than source opposition. As a consequence of this, once the inclination voltage is higher than the Coulomb barrier edge, an electron will swiftly burrow from the source burrow intersection to the island. However, due of the larger obstacle that the channel burrow junction presents, it will take a substantially longer amount of time to bypass, which will result in a nearer immersion of current and voltage characteristics. As a result, we are able to recognise the distinction between symmetric and topsy-turvy SET, which is characterised by the fact that an electron departs the island immediately after entering it in a symmetric device. Whatever the case may be, with the imbalanced device, an electron departs the island at the same rate as it enters it while it is inside.

**4. RESULTS AND DISCUSSION**

By taking into consideration the length and breadth that are appropriate, we have designed the single electron device so that it has two openings. The findings provide an assessment of the proportion of the disaster area that is affected. Through the process of reproducing the model, we were able to see the progression of the single electron from the source to the channel. In addition, we have the ability to comprehend the significance of charge transit from the source to the channel in relation to this.

Figure 5 is a graph that illustrates the drain current, IDi as well as the PC-based knowledge function of the gate voltage VG. It also illustrates the features of the drain current in relation to the gate voltage when the drain voltage VD is equal to 0.5V and 0.05V. As a component of the doorway voltage, the channel current, ID is shown in the schematic that can be seen in Figure 6. In order to demonstrate the qualification at these levels, the channel current's relationship to the voltage at VG=0.1V, 0.25V, and 0.5V is used. Characteristics that are essentially straight are shown at the doorway voltage of 0.5 V.

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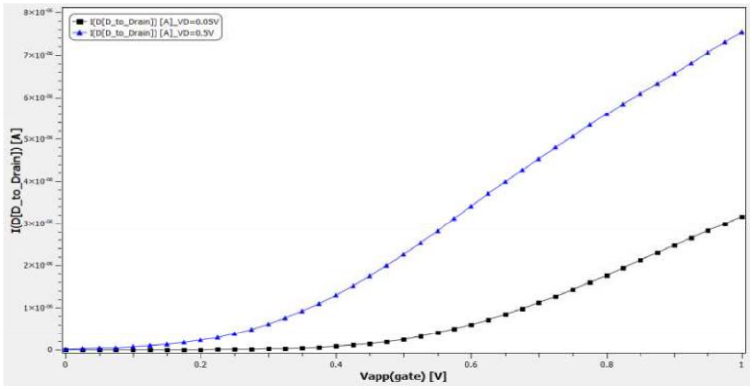


**Fig. 5 drain current, $I_D$ as a component of the gate voltage, $V_G$**

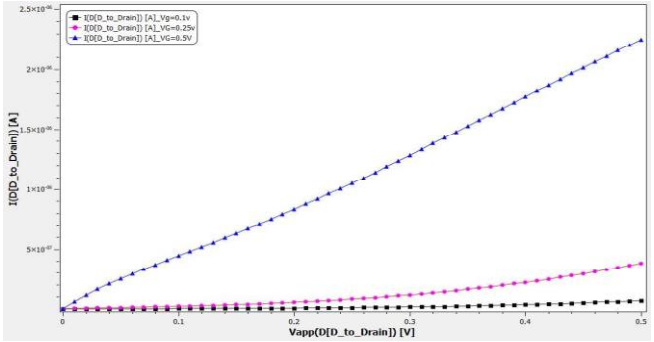


**Fig. 6 drain current, $I_D$ as a component of the drain voltage, $V_D$**

The channel current begins to increase abruptly at an applied voltage of 0.5V for the channel voltage, and a similar phenomenon to that of metal oxide semiconductors begins to take place for higher applied voltages. The electron portability is seen in figure 7. The purpose of this experiment was to determine whether or not there is a decrease in the number of electrons at the outer layer of the island at the beginning of the recreation, and whether or not the portability of electrons is more noticeable from the beginning of the recreation to the end of the recreation.

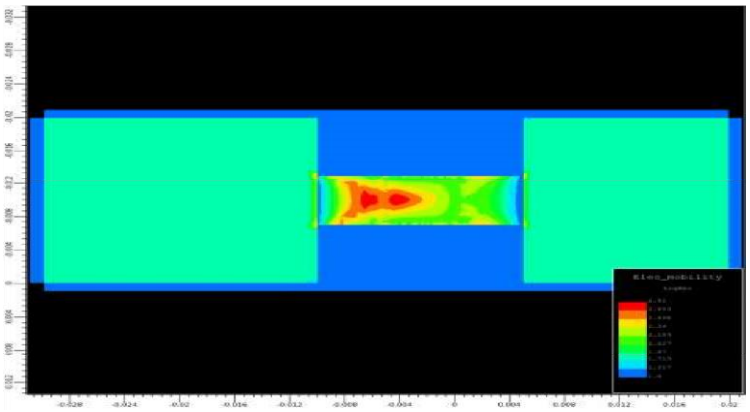

**Fig. 7 electron mobility**

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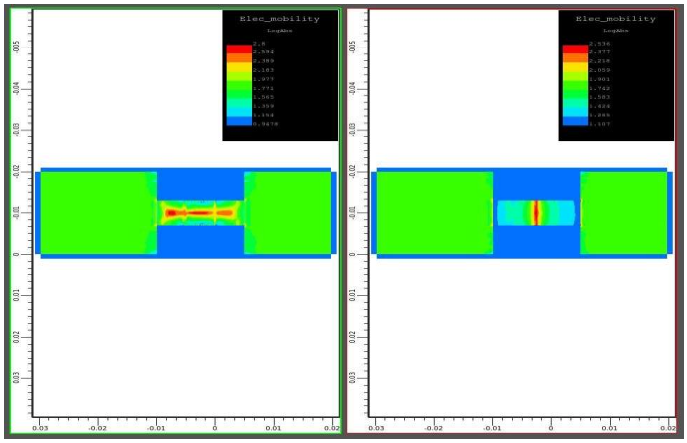

**Fig. 8 electron mobility at 300k**

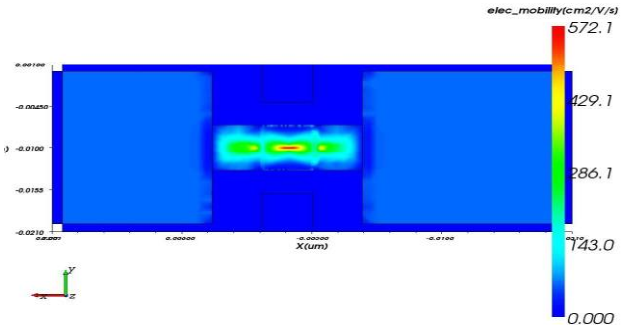


**Fig. 9 electron mobility at 100k**

The Fig. 8 shows the electron mobility at gate voltage $V_G$=2V and the drain voltage $V_D$ = 0.01V.The first part of Fig. 8 explains the initial position of the electron and the second part signifies the final position of the electron at temperature 300K. We tried to investigate that electrons are moved from the source to drain one by one. By taking the same parameter values, Fig. 9 signifies that at the temperature 100 K the electron

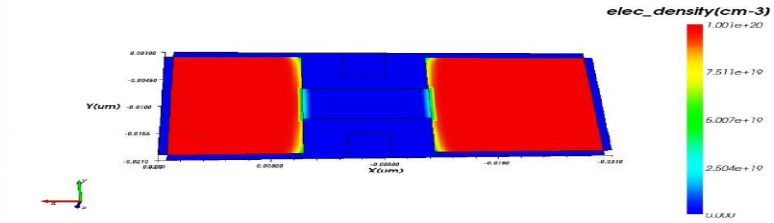


**Fig. 10 electron density**

mobility is less as compare to the electron mobility at 300K. Electron density is the amount that tells us how much charge is present at the drain point. Electron density is increasing when electron moves from the source to drain. Fig. 10 illustrates the density of electrons in the final stage and also demonstrates that red and yellow colors signify the presentation of the number of electrons at the end. Blue color shows the initial position of electrons. The electron density with cutline portrays that the electron density rises steadily as the injection of electrons increases at the source. Therefore the green line shows the density of electrons is higher as compare to the red line where the density of electrons is lower.

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From fig. it is also concluded that there is the small hill of electron density around the island and thereafter slow downfall in the density and increases steadily around the drain.

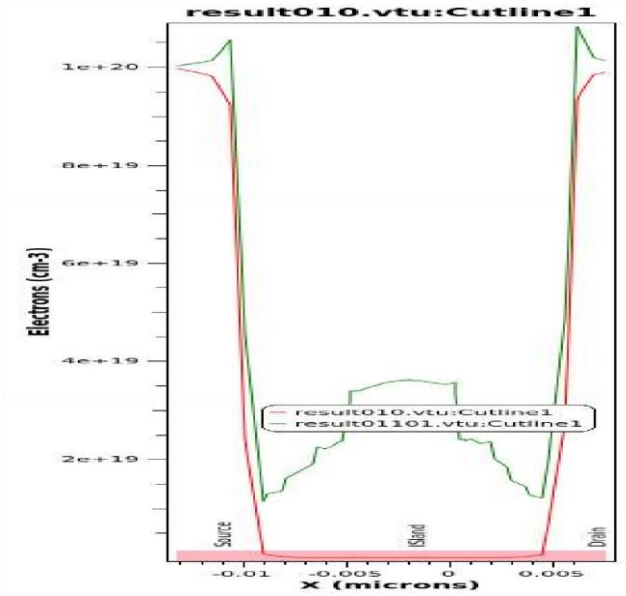


**Fig. 11 electron density using cut line**

Fig. 12 shows the electron density with the initial and final state. Since this picture shows two electron density surfaces, it tells us much more about the overall distribution of the electron than previous one. As seen in the figure below, using the higher number injected electron significantly increases the electron density.

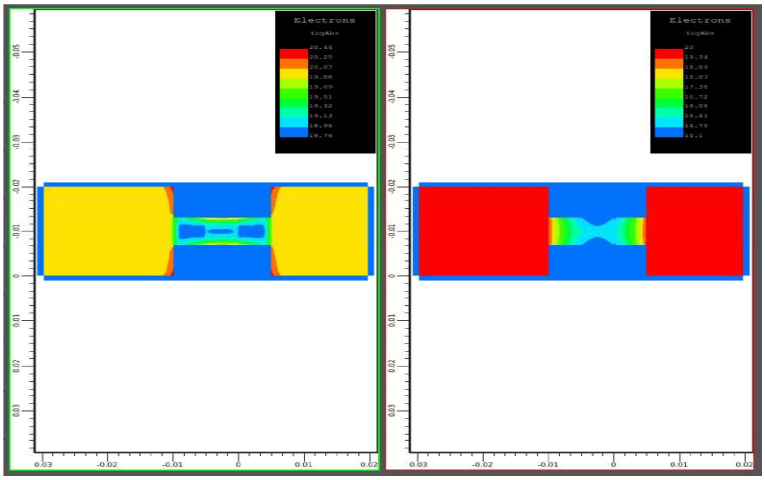

**Fig. 12 electron density with initial and final state**

In fig. 13, it is examined that at near to the ground field condition, the velocity of holes and electrons is directly relative to the electric field across the channel.

From fig. 14 and 15, it is concluded that at low electric field condition, the mobility of electrons is straightforwardly relative to electric field across the structure. The mobility of electrons in the final section is reasonably high, where the energy level for transfer of electrons is reduced. This leads to coulomb blockade effect in the single electron transistor. The carrier velocity at the drain area is comparatively high, where the energy level for the transport of electrons is reduced. This leads to coulomb blockade effect in the single electron transistor.

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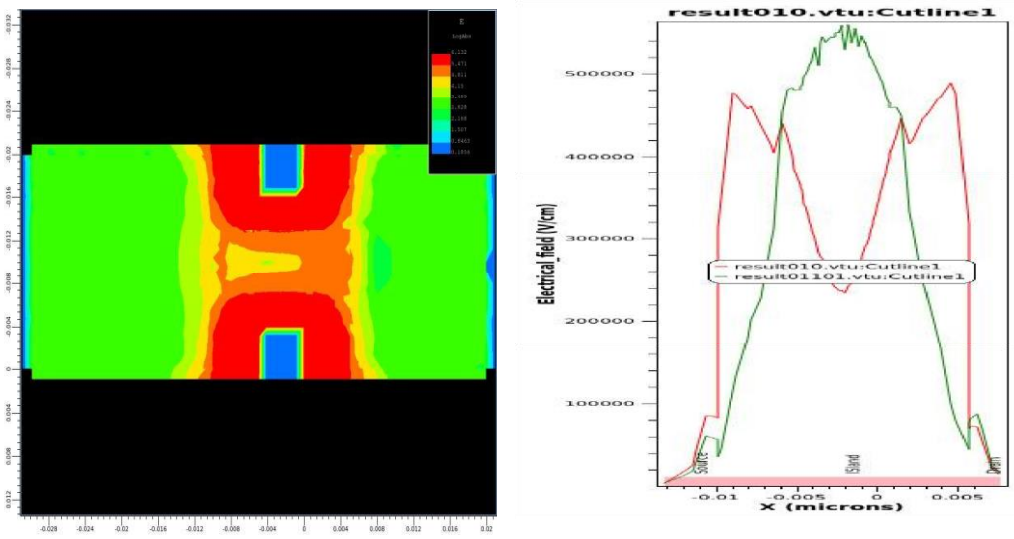


**Fig. 13 electric field and electric filed contour at the initial and final gate voltage**

When the electrons travel, they are concerned by the electric field formed by the gate voltage and hence they keep continue stunning and skipping against the exterior, as they pass through. Consequently the exterior mobility of the carriers is much reduced, in contrast to bulk mobility.

Fig.14 illustrated the electric effects on the threshold voltage with the electric field generated at the time of simulation which is shown at logarithmic scale. Underneath the applied electric field, remoteness of electrons and holes are greater than before, suggests the decrease of energy. It is more prominent when gate to source voltage is decreased. Lateral electric field increases with substrate doping concentration that reduces the threshold voltage of the device.

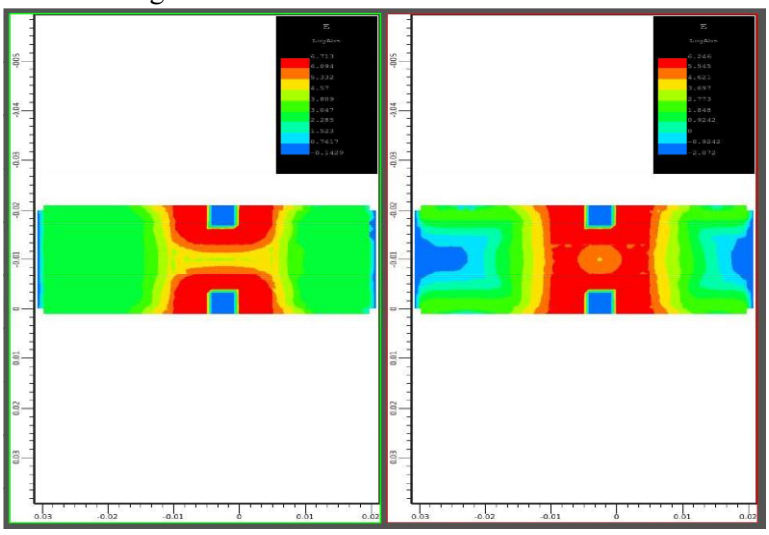

**Fig. 14 electric field at initial and final gate voltage**

Now, As the gate voltage is concentrated, the drainage grid increases, so the electric field made with the gate must be large than before proportionally. The stronger electric field of the gate increases the surface dispersion. So increased surface dispersion impacts the I-V characteristics of the transistor.

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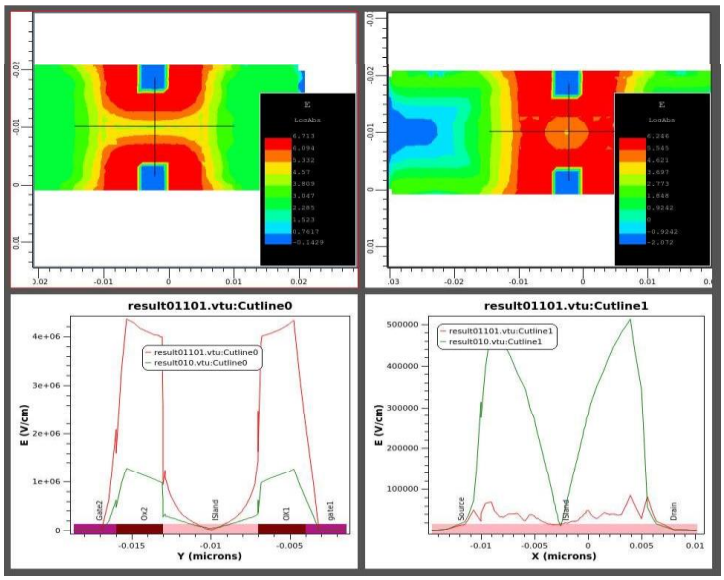


**Fig. 15 electric field contour at both temp**

Fig. 15 shows the electric field contours with the temperature at 100K and 300K. Fig. 16 shows the capability of the island can be prejudiced by a gate voltage by means of a capacitively coupled gate electrode of capacitance expanding the island potential prompts a down move of all island energy levels. In the single electron transistor, this strategy is utilized to conquer the Coulomb blockade and the transistor is flipped to its conductive state. The variation of gate voltage causes modification in potential in all regions which in turn decides the electron tunneling.

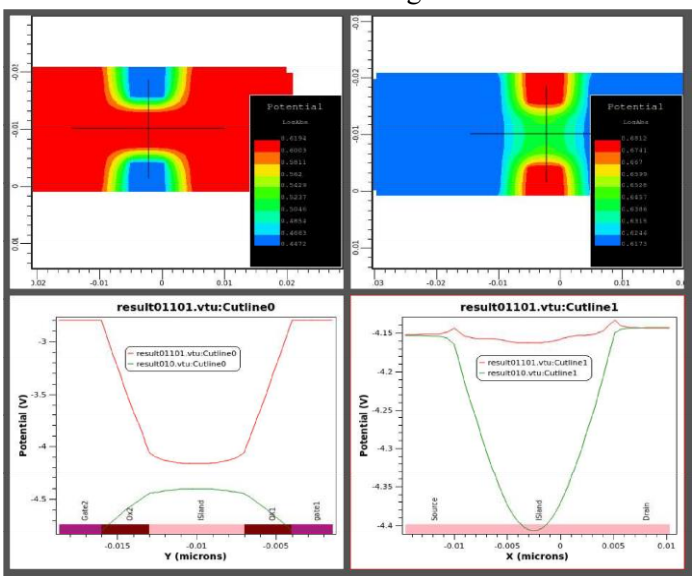


**Fig. 16 potential distribution**

The potential depends linearly on the gate voltage, though the aggregate energy demonstrates a quadratic reliance. In this way, the energy distinction between the potentials of various charge states stays steady for any connected voltages. Initially potential distribution only in the gate level which is visible with the red line curve resultant to a modification in the current. Next to the green line the capability of the island is allied at the drain.

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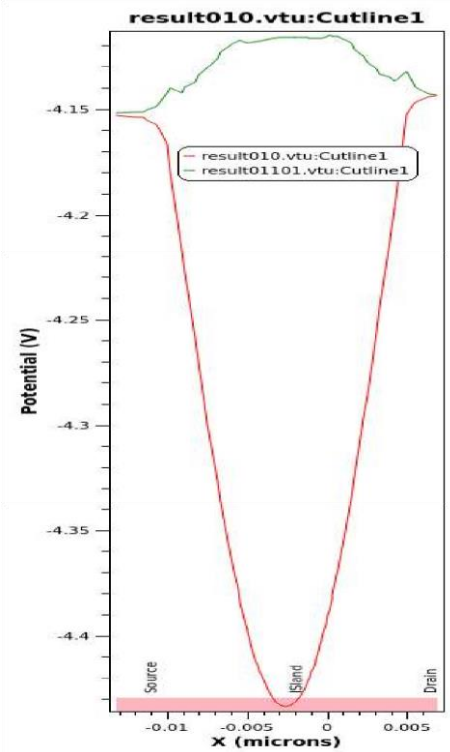


**Fig. 17 device potential contour at the initial and final gate voltage**

The type of potentials can be changed in a wide range, therefore the capacitances the size of the quantum speck and the coupling quality of channel contacts can fluctuate. The correct charging energy of abundance electrons is acquired by entirely coordinating the island potential over the overabundance charge. Fig. 17 shows the potential contour at the initial and final gate voltage.

Fig. 18 shows the flow of the electron in the device simulation. At the point when a predisposition voltage sufficiently remarkable to surmount the Coulomb Blockade is connected, current will pour through a single-electron transistor as the electrons tunnel on and off the island. For low bias voltages and temperatures, electrons tunnel, on the island from the source anode and then off the island to the drain anode each one in turn. best expression of the current can be accomplished when a single electron transistor is biased in this regime, so this is the most imperative case to consider for applications. On the other hand, the current within the Coulomb gap is considered to occur from the dissociation of thermally activated energy levels, which can move in response to a forced electric field.

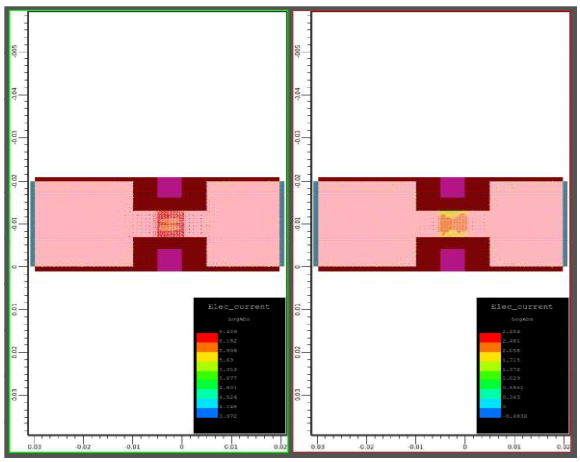

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**Fig. 18 electron current conduction**

We see that it gathers the condition expressed that the door charge should be one a portion of the worth of the charge of the electron as per the circumstances for current conduction through the SET. Assuming the entryway implicated is equivalent to whole number upsides of essential charge the Coulomb barricade will be dynamic and there will be no conduction. That is on the grounds that the framework has least energy when the island has a well unmistakable number of electronic charges and the burrowing of an electron will just build the widespread energy of the framework.

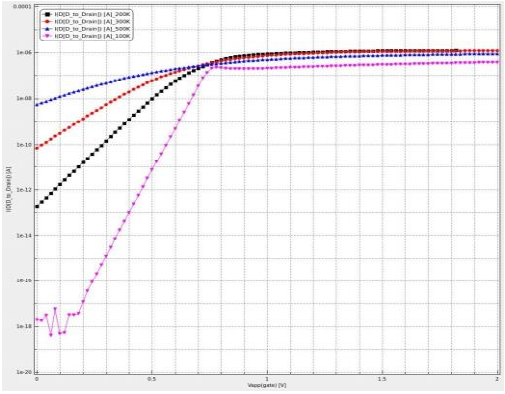

**Fig. 19 $I_D$ vs. $V_G$ plot for temperature variation at 100K, 200K, 300K and 500K**

Fig. 19 uses 10 mV to display the door voltage and channel current at various temperatures. SETs to work for the room temperature movement, the strong capacitance of the device expects a huge part. Devices with assortment in the source to exhaust openings are planned to grasp the impact of the amount of islands in the predominant driving manner lower to make a SET contraption worked at 300K which is a room temperature. In the figure it is shown that the continuous assortment of the laser voltage at different temperatures is shown in the figure. The grain stream is straightly changed at a temperature of 300K. The characteristics shows that most noteworthy channel current is seen for room temperature movement for instance 300K. As the not entirely set in stone at room temperature found shows that it is totally fit for room temperature action, the characteristics shows that generally essential current in like manner available at room temperature. The ambivalent nature is shown by the trademark. Gadget lead on both sides, acting as a p-type when channel voltage is positive and an n-type when channel voltage is negative.

So, ambipolar nature of device is observed. Tunneling is observed in both sides.

Table 2 shows the different off current values at the different temperatures .It is evident from the table that at low temperature off current is better.

**Table 2 Temperature vs. $I_{OFF}$ (Off Current)**

| IOFF | 100K | 200K | 300K | 500K |
|---|---|---|---|---|
| | 1.982 e-18 | 1.81 $e^{-13}$ | 6.937 $e^{-11}$ | 517 $e^{-9}$ |

Table 3 shows the different on current values at different temperatures. It is shown in the simulation that leakage component is less at 100K.

**Table 3 Temperature vs. $I_{ON}$ (On Current)**

| ION | 100K | 200K | 300K | 500K |
|---|---|---|---|---|
| | 3.807 $e^{-7}$ | 1.2 $e^{-6}$ | 1.21 $e^{-6}$ | 9.34 $e^{-7}$ |

linear regime is anticipated by taking the 1, 5 and 10mV for the different supply that strongly resembles the transfer characteristics reported in Fig. 20.

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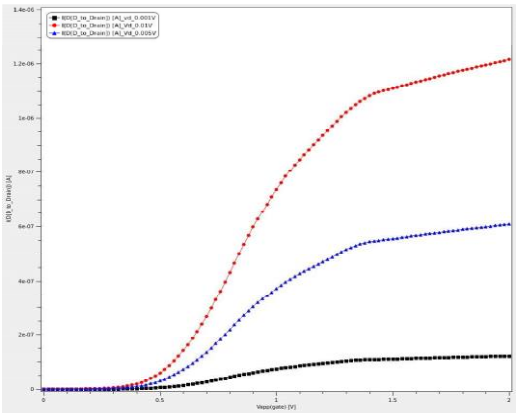

**Fig. 20 linear plot $I_D$ vs. $V_G$ (transfer characteristics) for the different drain supply at 1,5,10 mV**

To affirm that the contraptions are in the immediate framework at the related channel voltage (Vds), the yield characteristics of the device is displayed in Fig. 20. From the appraisal, unquestionably, the contraption shows the obvious straight framework with no indication of other restriction. It is clear from the plot that satisfactory amounts of electron are available to shape the channel. This shows the probability of current stream. The electron thickness plot shows that sufficient amounts of electrons are open to approach the channel. Figure portrays the gadget's voltage move trademark with different channel current qualities. 21. The voltage move qualities' inclination is used to register acquire.

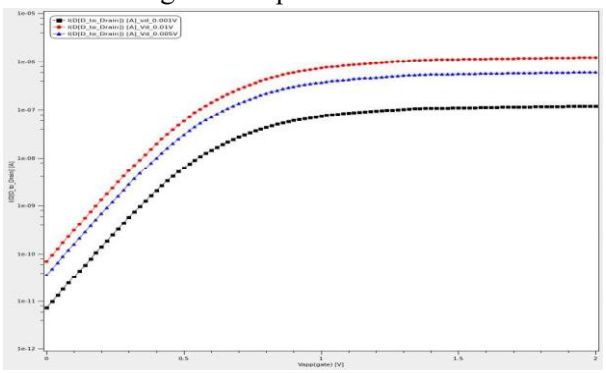

**Fig. 21 log plot for $I_D$ vs. Vg (transfer characteristics) for the different drain supply at 1,5,10 mV**

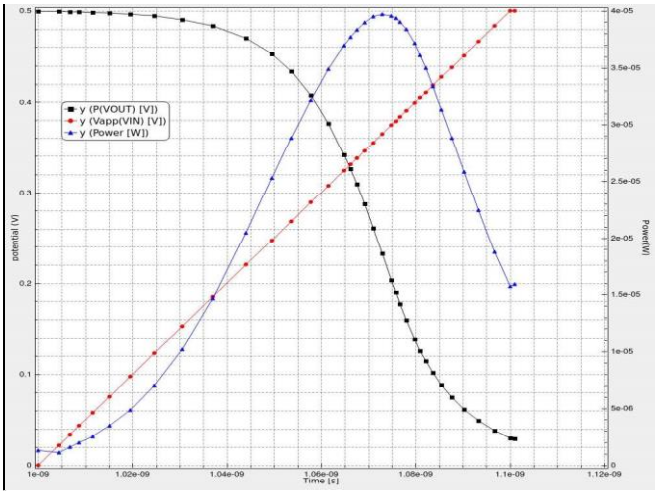


**Fig. 22 transient power characteristic**

Figure 22 shows the characteristics for power dissipation of an inverter. It shows the power consumption with corrosponding to input voltage and output voltage in a single plot. It shows maximum power is used during the state trasition of devices.Figure also shows the transient characteristics of power

dissipation. From the characteristics it is clear that maximum power is dissipated when SET are switching from one logic state to other. From figure, it is also clear that when input voltage has the maximum value of .5 V, maximum power get dissipated and when value of output voltage is .5 V then also maximum power get dissipated. Figure also illustrates that whenever the value of potential is .5 V maximum power is dissipated by the inverter.

**5. CONCLUSION**

An arrangement and reproduction of a single electron semiconductor with a signature kind channel growth of silicon oxide (SiO2) is carried out using Visual TCAD and Virtuoso Test framework. The semiconductor is then tasted at a temperature of 300 K at room temperature. It is necessary to have assortments in the source to exhaust openings in order to comprehend the influence of the amount of islands in the popular driving way, which is decreased. This is an essential need for smooth operation. As a result of the influence that the electric field has on the conduction band, the burrowing of electrons is also increased. This is shown by the fact that the door voltage rises immediately in conjunction with the field. An examination of the mimicked electrical features, such as the value of capacitance, the charging energy, and the power of SET for a fair entry voltage from the channel flow to the voltage outline, is carried out using the TCAD instrument. The capacitance that is seen in this entertainment is not as great as it was in the past, and the findings that were accounted for before indicate that the charging power is optimal in comparison to the past. At a temperature of 300 degrees Celsius, the threshold voltage for the SET device is 0.827 volts, and it is operated at room temperature. At 100 K, the spilling current that is seen in the entertainment at a variety of temperatures is more than at other temperatures.

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